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Architectural Considerations, Software Support and Compiler Issues in Multi-Computer Implementation

Final Report by

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1 Statement of Problem Studied

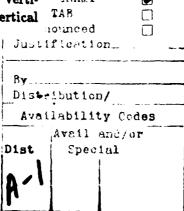
We have studied the problem of efficient execution of programs on parallel computers — and on the B-HIVE architecture in particular — and the software support required, concentrating on programming language implementation.

In a loosely-coupled multiprocessing environment, in which processors communicate over a generalized hypercube or similar network, the cost of sharing data among processes is quite high. We have investigated techniques of minimizing the total communication cost in parallel programs. We have also looked into ways of introducing parallelism in combanitorial problems and observed the impact of randomization on the system speedup. Besides the speedup, the network connectivity and data distribution in parallel & distributed systems play a very important role in determining the system performance. We have computed the reliability of such systems under different environment. In addition, we have studied the design of topologies with limited connections and which could be appropriate for both LAN & MAN applications.

2 Summary of the most important results

We are interested in techniques for arranging parallel code onto loosely-couple processors so as to minimize communication overhead and maximize processing speed. This is a synthesis problem, similar to the problem of optimization and code-generation in a traditional compiler. It is very different from the analysis problem of discovering potentially parallel operations in the program. Much previous research has centered on designing programming languages that express parallelism explicitly, and on program analysers that discover implicit parallelism in sequential codes. Our work is independent of these issues and compatible with either approach.

We use a medium grain parallelism model to minimize communication overhead [1-10]. A medium grain model is shown to be an optimum way of merging fine grain operations into parallel tasks such that the parallelism obtained at the small grain level is retained and communication overhead is decreased. Our "vertical partitioning" and scheduling techniques have been evaluated by the simulation of ten EISPACK subroutines [7]. The vertical partitioning model clearly outperforms the model without the vertical partitioning.



A new communication model has been introduced [1], allowing additional overlap between computation and communication. Simulation results indicate [8] that the medium grain communication model shows promise for automatic parallelization for a loosely-coupled multiprocessor system.

Since most of the computation in a program is performed inside loops, parallelization of loop structures is an important topic and has been extensively studied in the past. The particular program of loop execution on a loosely-coupled parallel processor has not received much attention, however. We introduce a compensated loop scheduling that adjusts to the delays involved in distributed data for parallel execution. We also propose a nested loop scheduling that allows heterogeneous loop allocation [11]. Heterogeneous loop allocation adjusts to dependencies within loops and in some cases permits better utilization of processors in the inner loops. Additional experimentation [12] has been done to do parallel recursive least squares computation in distributed memory multiprocessors. All these problems have been studied for efficient execution of programs on parallel computers in general, and on the B-HIVE architecture [13,14] in particular. We have shown that for some optimization problems, such as backtracking [15], and branch and bound [16], a randomized search algorithm yields high performance on a parallel processor. A major advantage of randomized search is that very little interprocessor communication is required.

There are many other factors that influence the performance of a parallel system. The impact of single faults on the system performance of a class of cluster-based multiprocessors have been considered in [17]. The effect of network connectivity and data distribution on various reliability and performance parameters have been studied in [18-21]. A comparison of various fault-tolerant multistage interconnection networks, has been performed in [22,23]. The requirements of LANs and MANs in terms of connectivity, are different than a general parallel systems and appropriate topologies for such doubly connected multidimensional networks and their characteristics, have been covered in [24-27]. Thus, the research results encompasses more than the areas just described in the proposal.

3 List of all publications and technical reports

1. J.-S. Leu, "Strategies for retargeting of Existing Sequential Programs for Parallel Processing," Ph.D. Thesis, N.C. State University, July 1987.

- 2. J.S. Leu and D.P. Agrawal, "Automated Task Decomposition Strategies for Multiprocessing," Tech report.
- J.S. Leu, D.P. Agrawal and J. Mauney, "Modelling of Parallel Software for Efficient Computation-Communication Overlap," Fall Joint Computer Conference, Oct. 1987, pp. 569-575.
- D.P. Agrawal, et al, "Strategies for Retargeting of Existing Programs," Invited presentation, Workshop on Parallel Processing, Oregon State University, June 1-2, 1987.
- 5. S. Hand and J. Mauney, "Compilation and Code Generation for multiprocessor computers," Proc. Southeast Conf., 1987, pp. 102-105.
- D.P. Agrawal, J. Mauney, and L.T. Simpson, "Structure of a Parallelizing Compiler for the B-HIVE Multicomputer," EUROMICRO '88, pp. 79-84.
- 7. D.P. Agrawal el al, "A Parallelizing Compiler for Supercomputing and its performance with Eispack," Tech. Report.
- 8. J. Leu, D.P. Agrawal, and J. Mauney, "Optimal-grain model in minimizing interprocessor communication for multiprocessors," ComCon88, Baton Rouge, Louisiana, October 1988.
- S. Kim, D. Agrawal, J. Mauney, "Parallel Loop Allocation on Looselycoupled multiprocessors," submitted to International Conference on Parallel Processing.
- 10. D.P. Agrawal, S. Kim, J.S. Leu, J. Mauney, "Modeling techniques in a parallelizing compiler for the B-HIVE multiprocessor system" submitted to International Journal of High-speed computing.
- 11. J. Mauney, D.P. Agrawal et al, "Computational Models and Resource Allocation for Supercomputers," IEEE Proceedings (submitted for publication).
- 12. S.Kim, D.P. Agrawal, and R.J. Plemmons, "Recursive Least Squares Computation on Distributed Memory Multiprocessors," Journal of Parallel & Distributed Computing, 1989 (accepted for publication).

- W.B. Wike, T.K. Miller and D.P. Agrawal, "Alpha Structure Based B-HIVE Multi-computer," Proc. Second Conf. on Hypercube Multiprocessors, Sept. 29- Oct. 1, 1986, SIAM, pp. 265-270, Knoxville, TN.
- 14. D.P. Agrawal et al, "B-HIVE: Hardware and Software for an experimental Multiprocessor," Technical report.
- 15. V.K. Janakiram, D.P. Agrawal, and R. Mehrotra, "Randomized Parallel Algorithms for Prolog Programs and Backtracking Applications," Proc. Int. Conf. Parallel Processing, Aug. 1987, pp. 901-908, also appeared in IEEE Transactions on Computers, December 1988, pp. 1665-1676.
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- I.O. Mahgoub and D.P. Agrawal, "Impact of cluster network failure on the performance of cluster-based Supersystems," Proc. 1986 Int. Conf. on Parallel Processing, Aug. 19-22, 1986, pp. 743-749.
- 18. S.Rai and D.P. Agrawal, "Reliability of Program Execution in a Distributed Environment," Technical report.
- A. Kumar, S. Rai, and D.P. Agrawal, "Reliability Evaluation Algorithms for Distributed Systems," Proc. IEEE INFOCOM '88, March 29-31, 1988, pp. 851-860.
- Y.K. Choe, D.P. Agrawal, and C.R. Green "A Hierarchical Message Mechanism for distributed Systems Software," Proc. Workshop on Future Trends of Distributed Computing Systems in the 1990, Sept. 14-16, 1988, Hong Kong.
- A. Kumar, S. Rai, and D.P. Agrawal, "On computer communication network reliability under program execution constraint," IEEE Journal on Selected Areas in Communations, Vol. 6, No. 8, pp. 1393-1400, Oct. 1988.
- 22. D.P. Agrawal, S.C. Kim, and N.K. Swain, "Analysis ans design of nonequivalent multistage interconnection networks," IEEE Trans. Computers, vol. C-37, no. 2, Feb. 1988, pp. 232-237.

- 23. G.B. Adams, D.P. Agrawal, and H.J. Siegel, "A survey and comparison of fault-toletant multistage interconnection networks," IEEE Computer, vol. 20, no. 7, July 1987, pp. 14-27.
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- 27. T.Y. Chung, S. Rai and D.P. Agrawal, "A routing scheme for datagram and virtual circuit services in the MSN," Proc. Phoenix Conference on Computers and Communications, March 22-24, 1989 (to appear).

4 List of all participating scientific personnel

4.1 Faculty

- 1. Dr. Dharma P. Agrawal
- 2. Dr. Jon Mauney
- 3. Dr. Suresh Rai (visiting)

4.2 Graduate Students

- 1. Mr. Ja-Song Leu, completed Ph.D., July 1987.
- 2. Mr. V.K. Janariram, completed Ph.D., April 1988.
- 3. Mr. A. Kumar, doctoral student, expected to finish in Summer 1989.
- 4. Mr. Sukil Kim, doctoral student, expected to finish in Summer 1989.
- 5. Mr. T.Y. Chung, doctoral student, expected to finish in Summer 1989.
- 6. Mr. Steve Hand, finished M.S. in 1987.
- 7. Mr. I.O. Mahgoub